WAFER
SCALE
MEMORY

5

6

MEMORY BUS
(HIERARCHICAL BUS)

MEMORY BUS/
INTERFACE

8

MEMORY
CONTROLLER

7

SYSTEM BUS
INTERFACE

9

4

SYSTEM
BUS

CPU

3

DMA
CONTROLLER

2

GRAPHICS
CONTROLLER

1

FIG. 1

M — Module

CTL — Controller

CTL — Possible Site for Controller

FIG. 2

BUS SEGMENT #3

FIG. 3

——————Conducting Layer 1

——————Conducting Layer 2
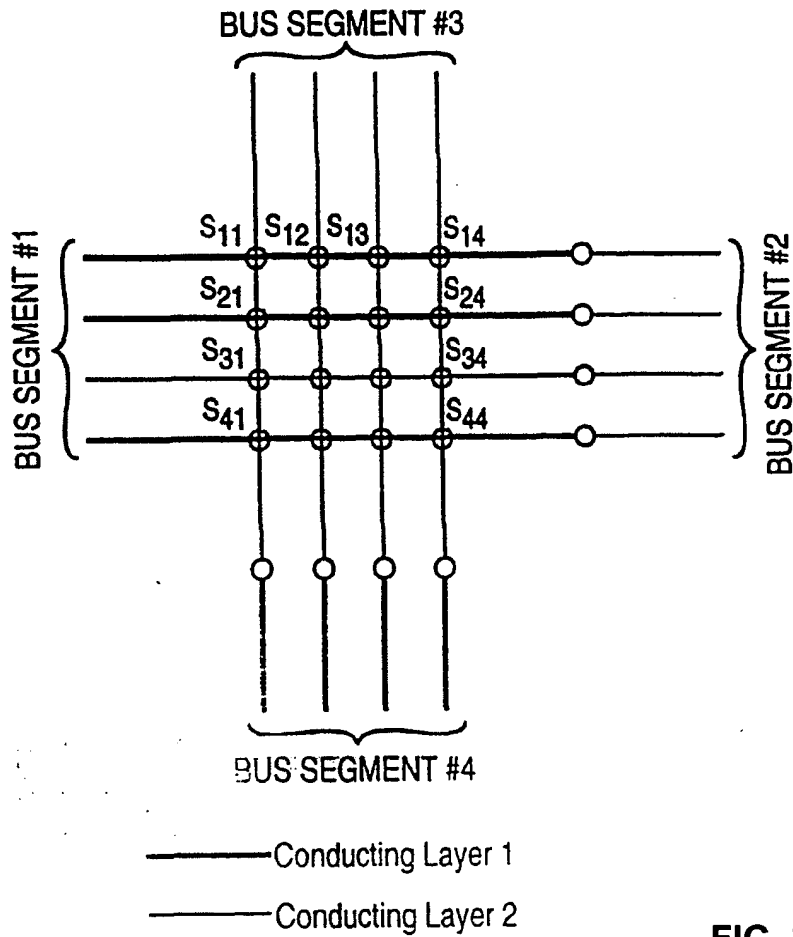
Group 1 - Block-mode transfer signals
- Bus Data [0:8]
- Clk

Group 2 - Asynchronous control signals
- Bus Busy   (BB#)
- Transmit / Receive   (T / R)
- TriState Control   (TC#)

FIG. 4

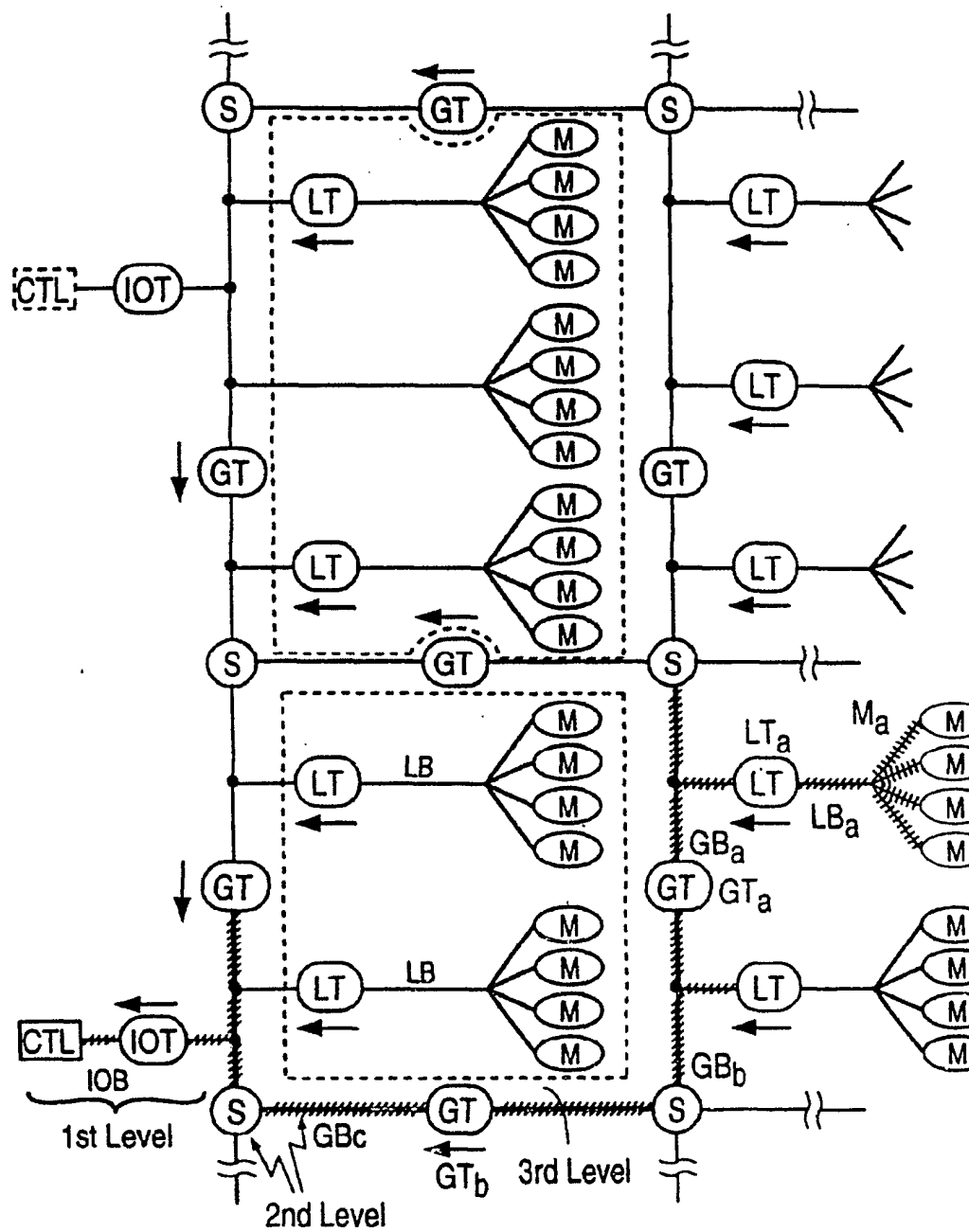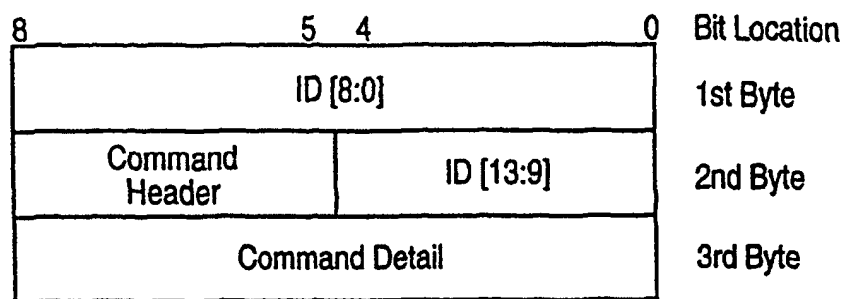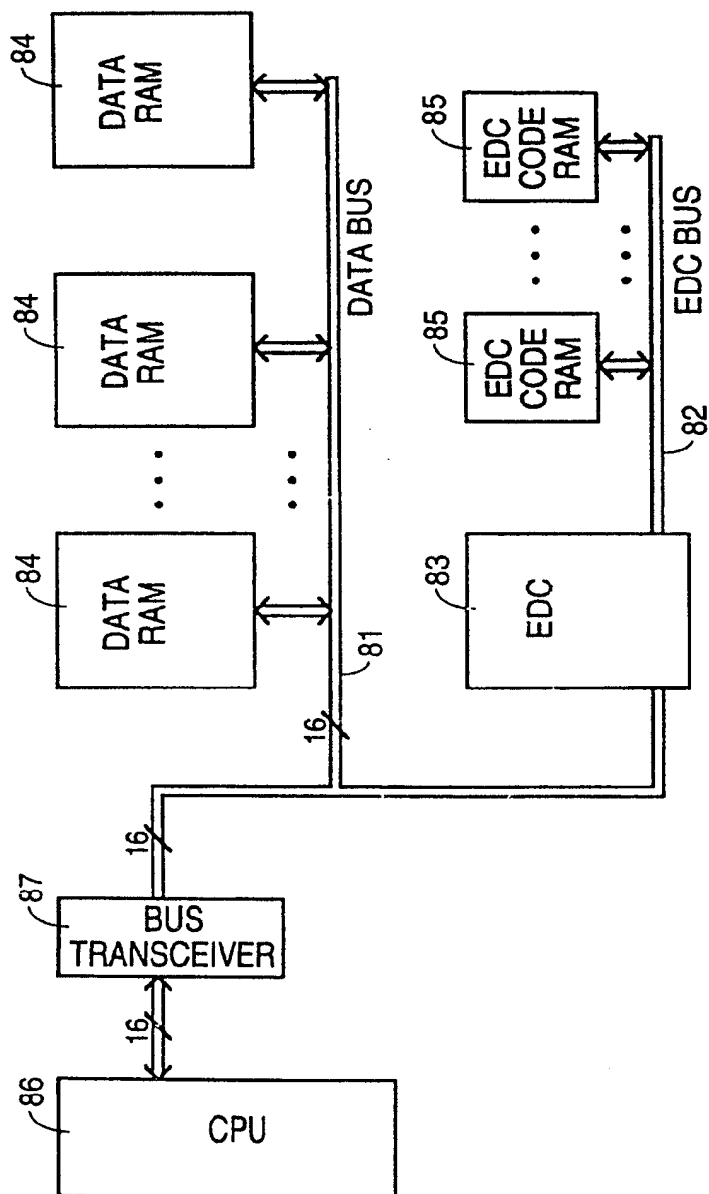| BB#	T/R	TC#	BUS STATE
0	0	0	Hi Z
0	0	1	Receive
0	1	0	Hi Z
0	1	1	Transmit
1	0	0	
1	0	1	Idle
1	1	0	
1	1	1	

FIG. 5

M — Module

CTL — Controller

CTL — Possible Site for Controller

FIG. 6

8	5	4	0	Bit Location
ID [8:0]				1st Byte
Command Header		ID [13:9]		2nd Byte
Command Detail				3rd Byte

FIG. 7

FIG. 8

BIT LOCATION 0   7 8

BYTE 0	D_0 D_7	ED_0
BYTE 1	D_8 D_9	ED_1

•
   •
   •
	•
	•
	•
		•
		•
		•

BYTE 8	D_{56} D_{63}	ED_7

DATA   EDC CODE

FIG. 9

FIG. 10B

FIG. 10A

FIG. 11

FIG. 12A

Clk

En

B101

M101

tck

DB0[n]

DB1[n]

dck

En

B100
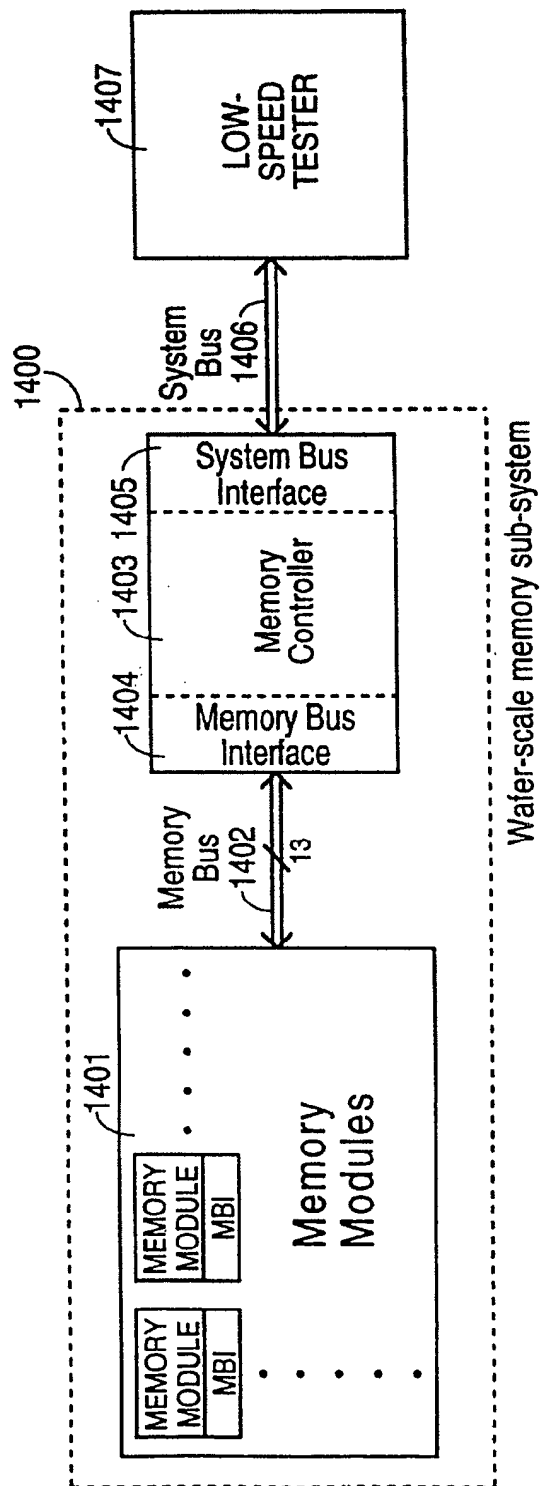
M100

Bus Data [n]

n = 0 to 8

tck

dck

clk

BusData [n]
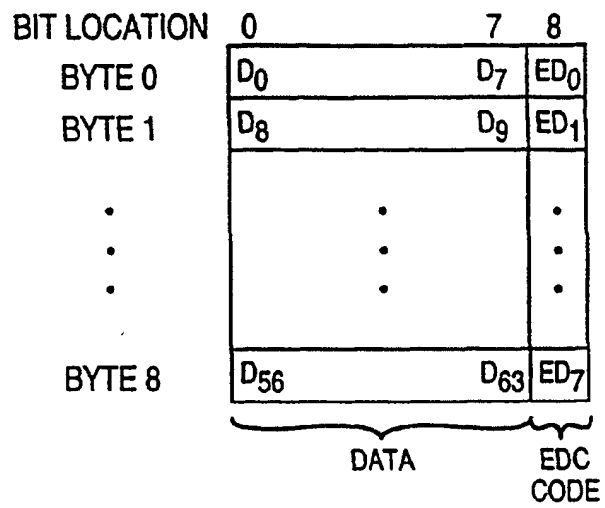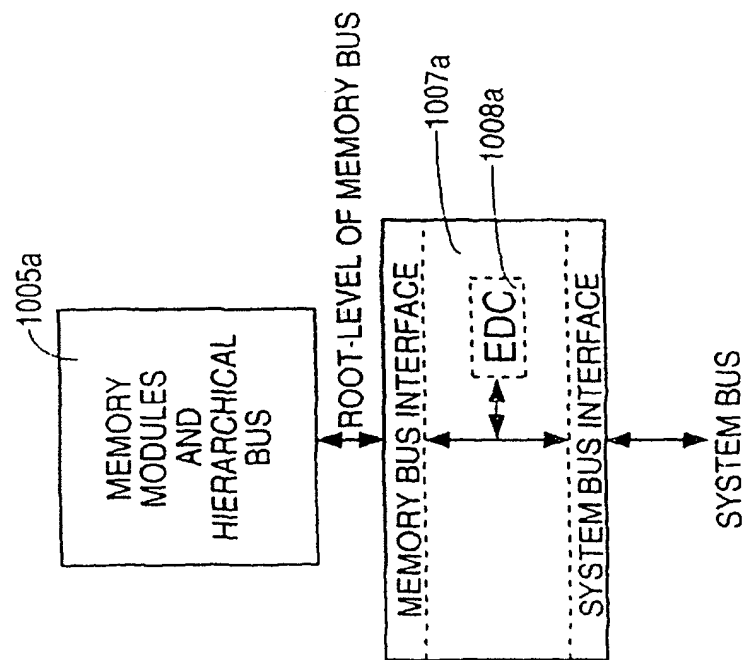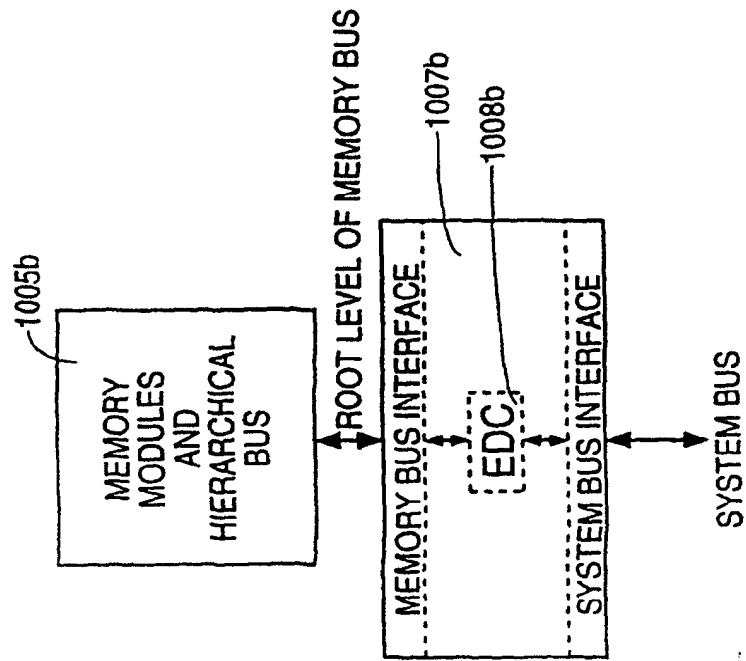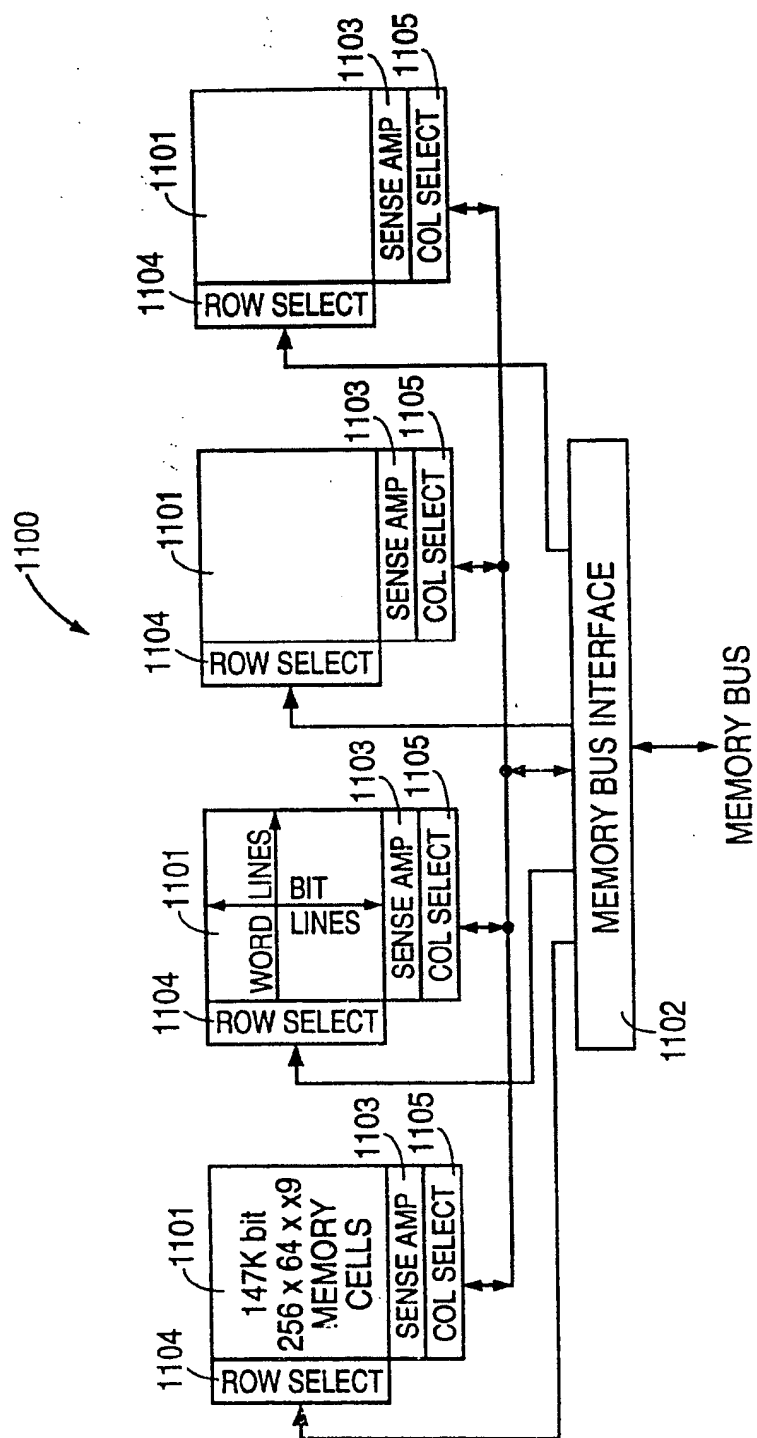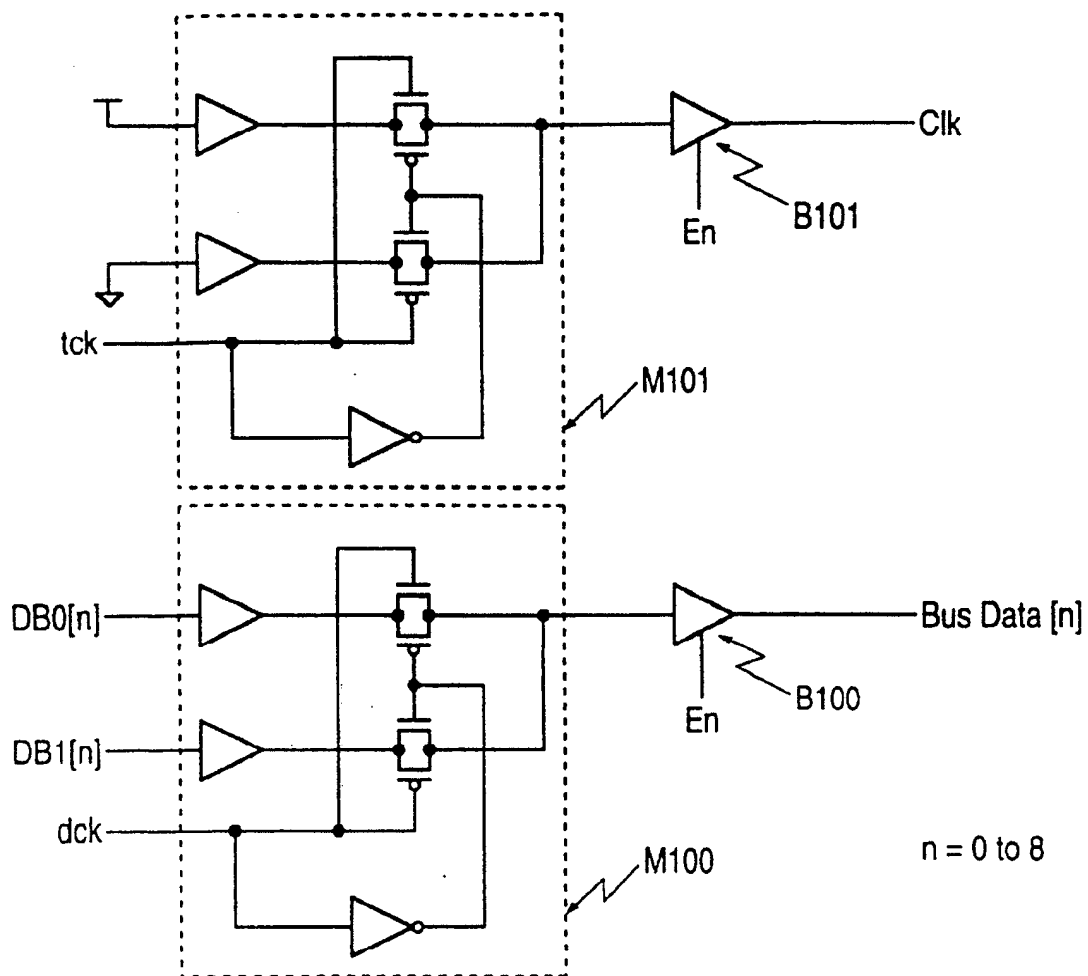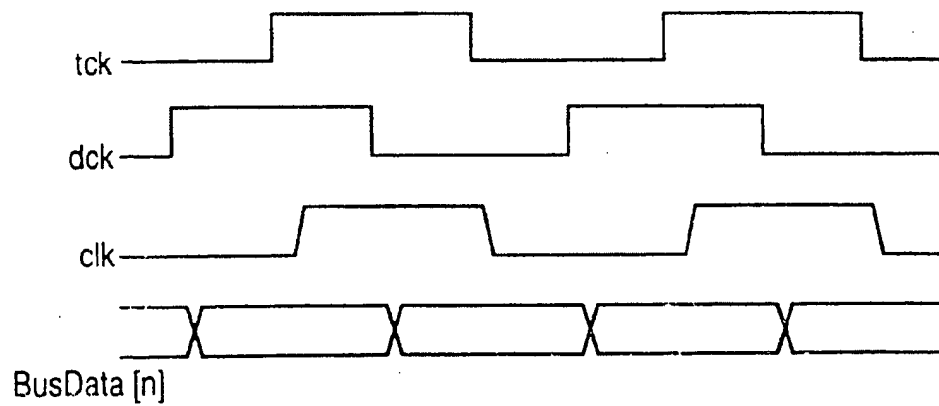
FIG. 12B
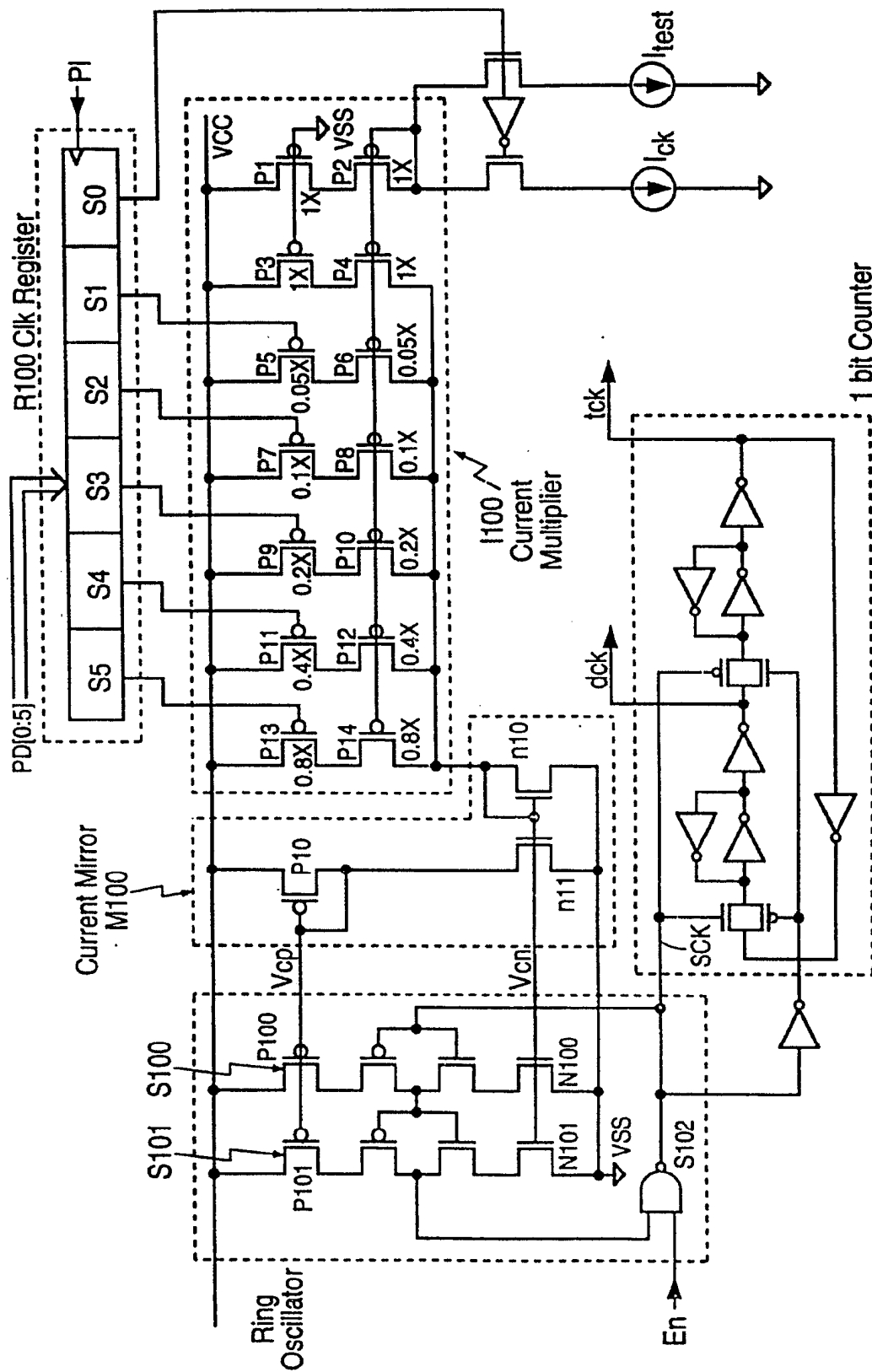
FIG. 13

FIG. 14

MBI = Memory Bus Interface

FIG. 15

```
         8    7    6                    0
       ┌────┬────┬────────────────────────┐
       │ S/L│ S/A│     BYTE LENGTH         │
       └────┴────┴────────────────────────┘
          ▲    ▲
          │    │      ⎰ 0 - ACTIVE
          │    └──────⎱ 1 - SPARE
          │
          │          ⎰ 0 - SHORT CACHE LINE  (64 BYTE)
          └──────────⎱ 1 - LONG CACHE LINE  (128BYTE)
```
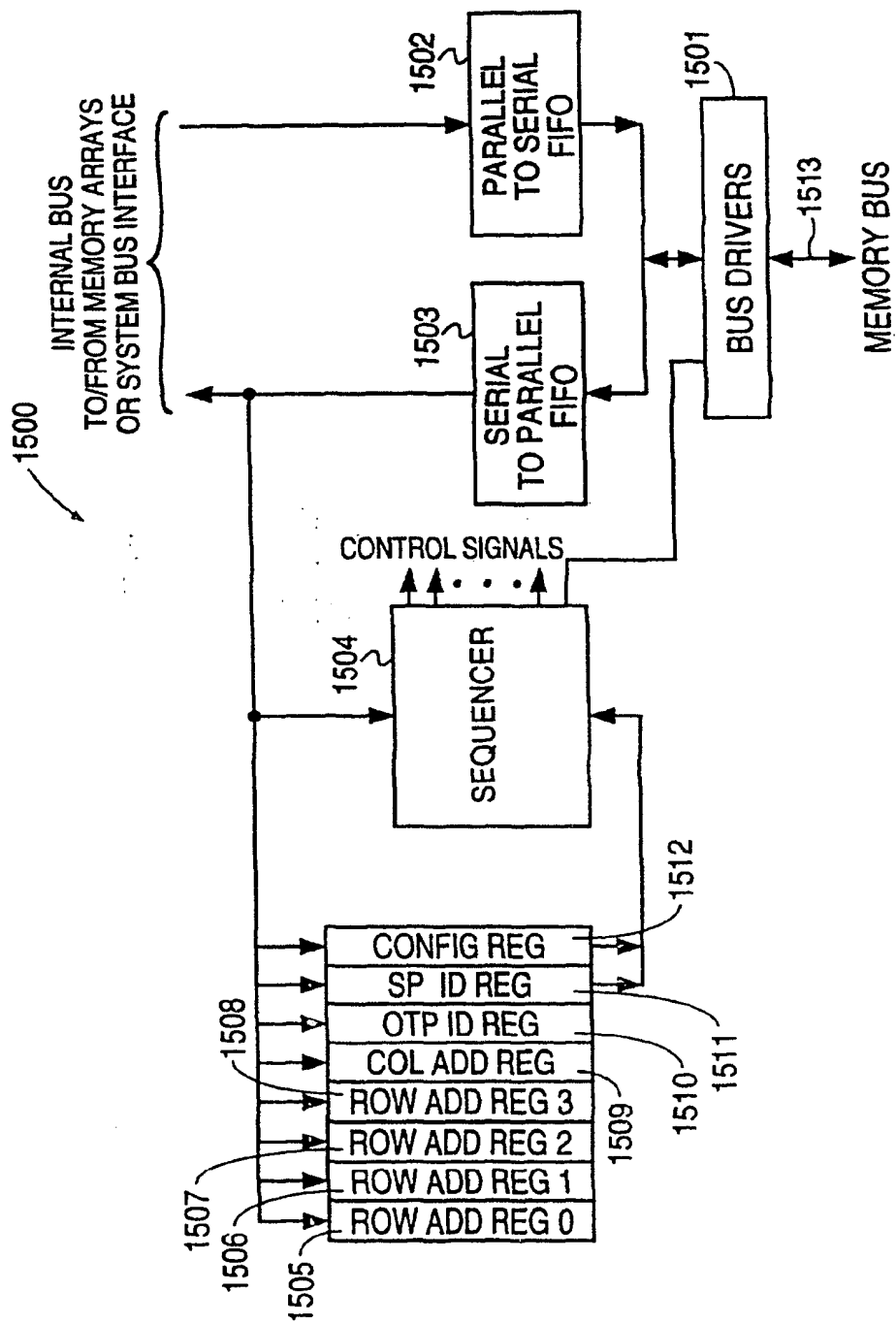
FIG. 16
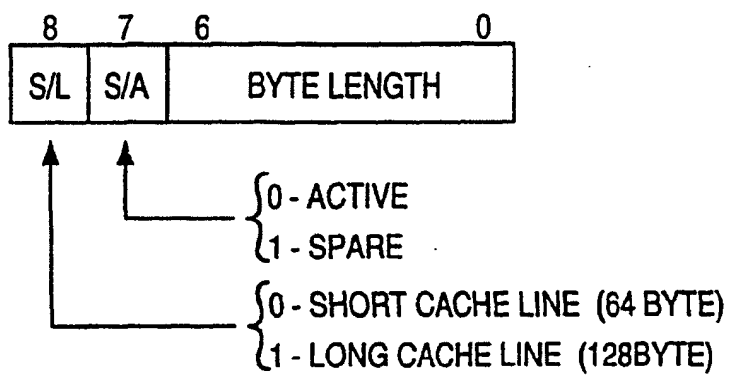
FIG. 17A
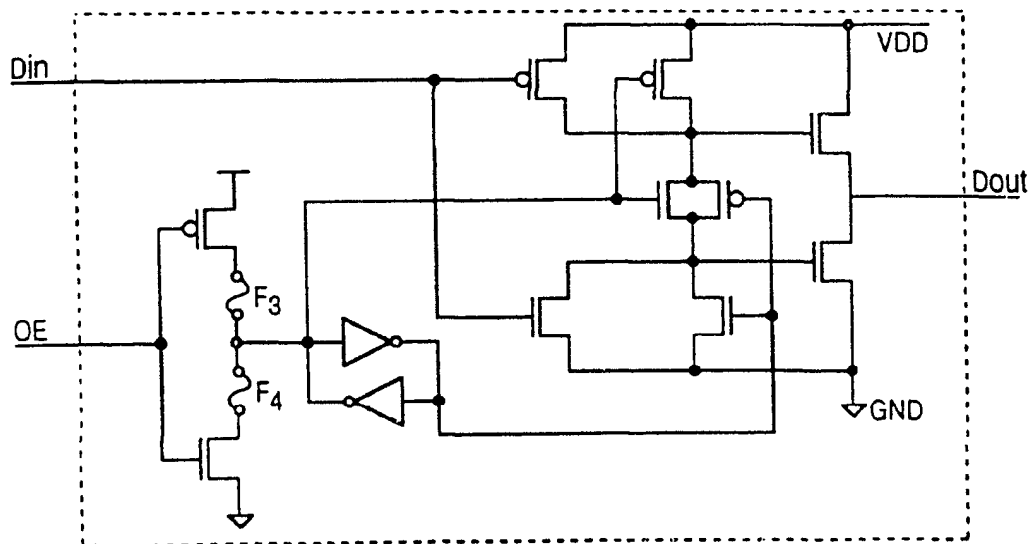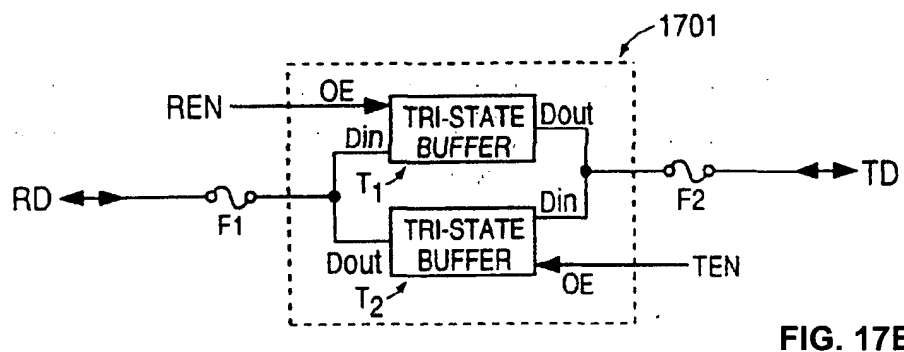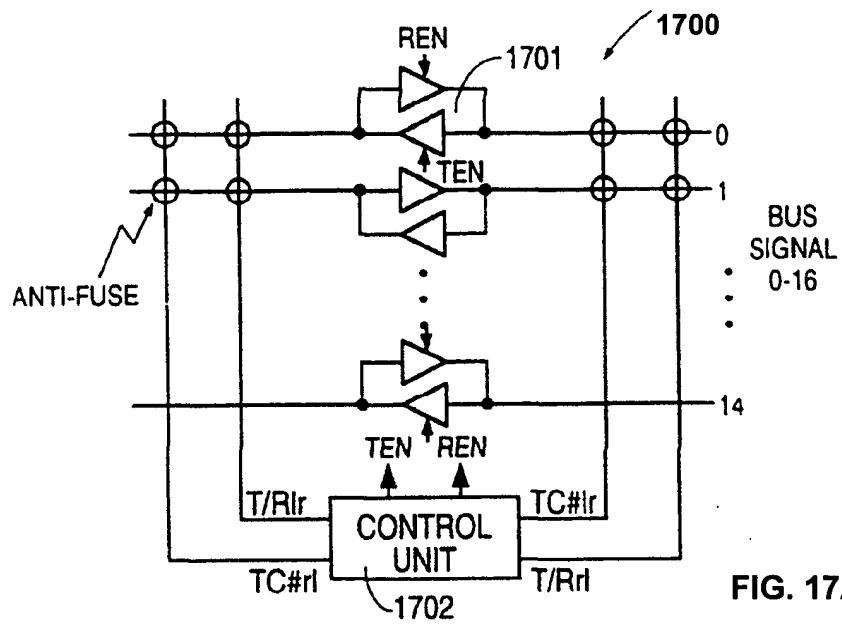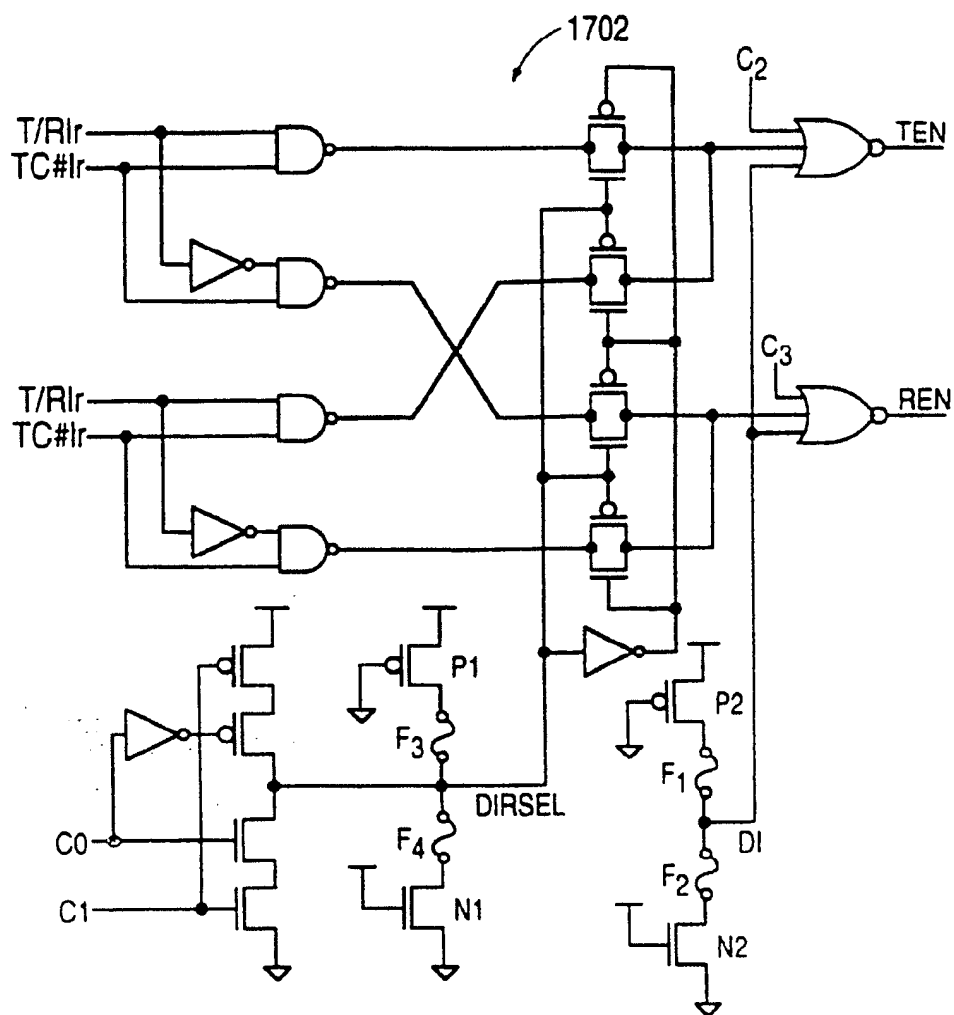
FIG. 17B
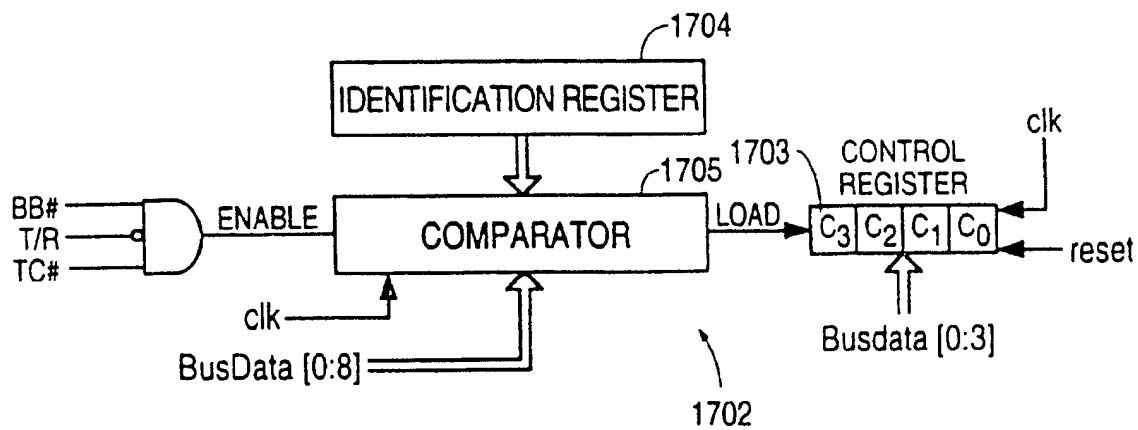
FIG. 17C

FIG. 17D

FIG. 17E
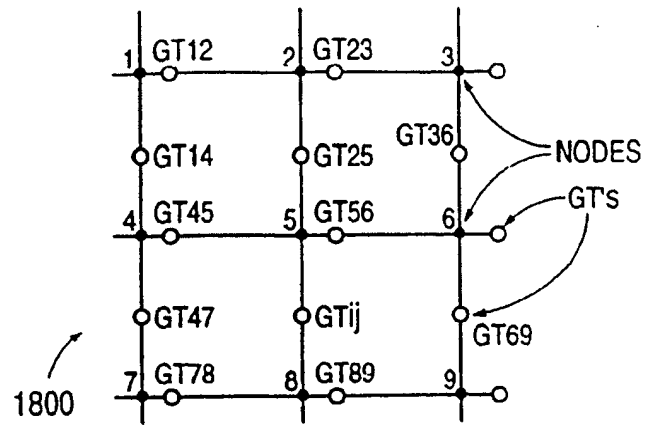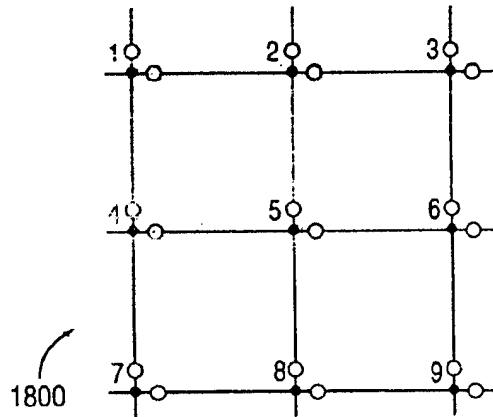
FIG. 18A

FIG. 18B
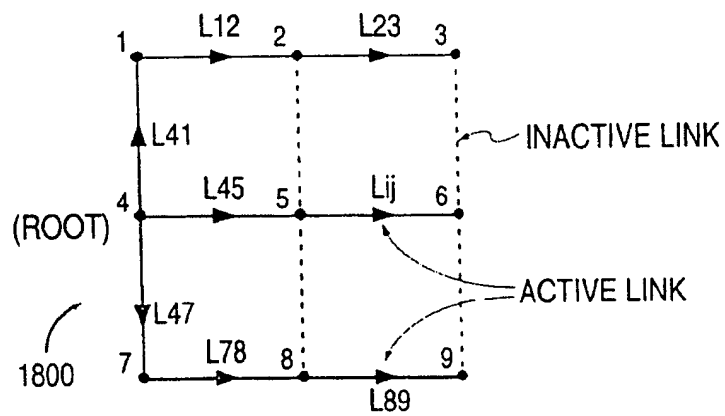
FIG. 18C
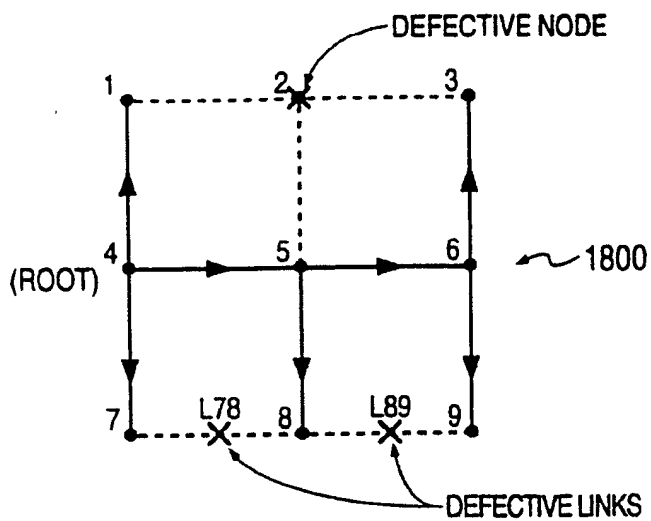
FIG. 18D

FIG. 18E

FIG. 18F

FIG. 18G